

Fujikura
Wafer Level Chip Sized Package
(WLCSP)
Design Guide

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 (without the Resin Post)

1. Introduction

Fujikura's wafer level packaging service is a foundry service of semiconductor components assembly and fabrication, which Fujikura processes package structures on the surface of wafers that customers provide, and returns them at wafer level to the customers.

Fujikura offers low cost and high reliable packaging technologies, which are combination silicon planer processes and additive circuit forming techniques. Fujikura has cultivated those technologies through developments and high volume productions of MEMS components and Flexible Print Circuit (FPC).

This design guide describes specifications of wafer that Fujikura can handle in the processes, design and process rules and finish specifications after the processes.

Because this design guide may not catch up with the leading edge of technologies making steady progress, there is a possibility that Fujikura can accept beyond the specifications and rules now.

Please consult with a Fujikura application engineer who takes charge of your project about your requirements. 'Quick & Flexible' is our basic policy.

Please find attached Appendix 1, 'Fujikura Wafer Level CSP Specification Chart'.

If the customer fills the blanks that are required, and submit it to the application engineer in advance, it will be appreciated.

The reliability after the wafer level packaging depends on its dimension at each of parts, thickness or other designs.

There is no all-round reliability data that can represent every package design.

Please note that required reliability tests should be done for every different model.

2. Available Structure

There are two types in Fujikura's wafer level packaging service.

One has Cu rerouting from the final metal I/O pads of the die to solder bumps.

The other has no rerouting and has only Under Bump Metallurgy (UBM) on the final metal I/O pads, underneath the solder bumps.

And a structure that has stress relieving resin posts underneath the solder bumps is an option for only design that has the rerouting.

The patent of the design with the resin posts has been applied jointly with Japan Texas Instruments Ltd.

Fujikura will be able to negotiate with customers who wish for the license after Fujikura takes the right.

2.1. Rerouting

Fig.1 is the cross section diagram for the structure has no rerouting.

Fig.2 shows the design with the rerouting.

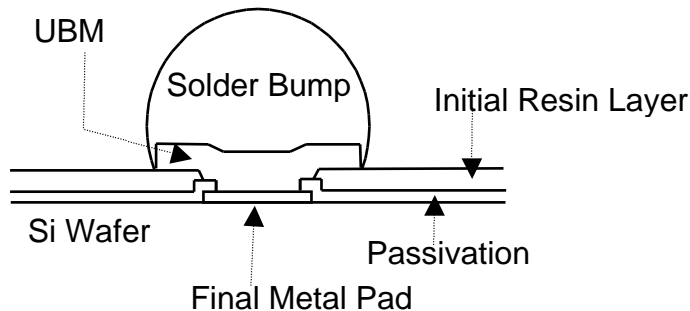


Fig.1 Schematic cross-sectional view of direct solder bump design.

In the design without the rerouting, there is the initial resin insulation layer with opening on the final metal I/O pads. The pads are covered with Under Bump Metallurgy (UBM), which are composed of seed layers and Cu plated layer, and solder bumps are formed on the UBM.

In the design with the rerouting, it connects from the resin opening on the final metal I/O pads to any points with seed layers and Cu plated layers. The overcoat lies on the rerouting and is opened at the point where solder bumps will be formed.

The seed layer works as adhesive material between the initial resin layer

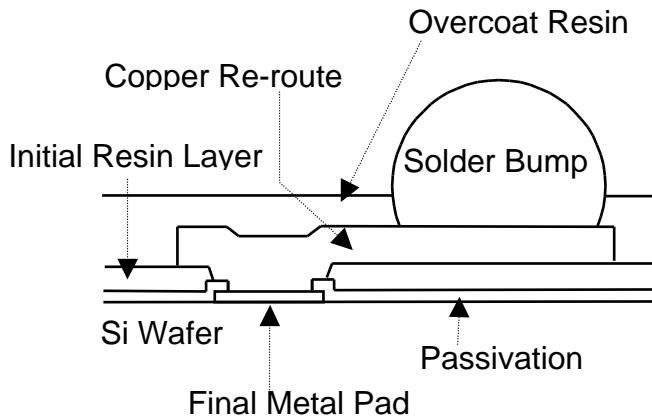


Fig.2 Schematic cross-sectional view of re-routed solder bump design.

And the Cu plating layer and as barrier metal between the final metal and Cu plating layer at the same time.

Overcoat resin is not only the sealing encapsulation but also the solder resist that defines bump forms.

2.2. Resin Post

Fig.3 is the cross section diagram of the structure has the stress relieving resin posts underneath solder bumps.

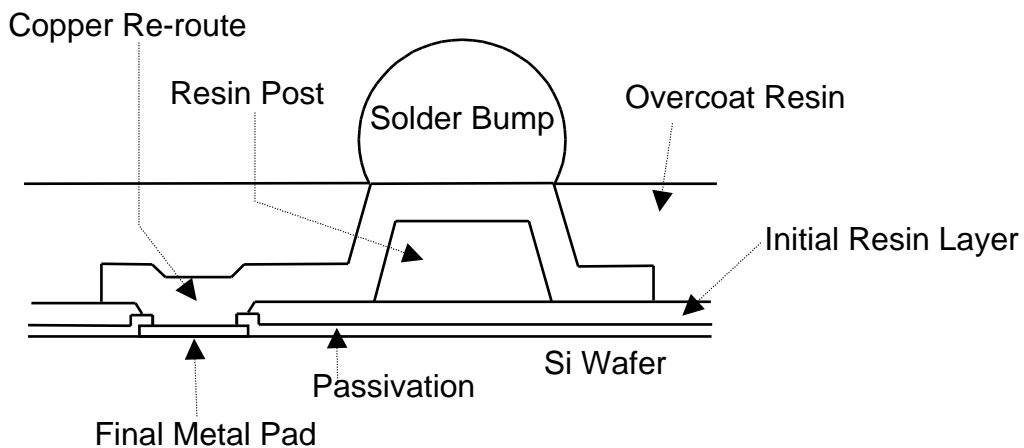


Fig.3 Schematic cross-sectional view of re-routed solder bump on resin post design.

In this design, there is the initial resin insulation layer with opening on the final metal I/O pads and resin posts where solder bumps will be formed. And then, the rerouting connects from the resin opening to the top of the resin post. Overcoat resin lies on the rerouting and is opened at the

post tops. Finally, solder bumps are formed at the opening of the overcoat.

3. IC/Wafer Specification & Design Requirement

This section describes specifications of wafers and dice, which Fujikura can handle in the wafer level packaging service.

The processes themselves and the reliability after the processes depend on die or wafer finish specifications.

Providing a few scrap wafers that Fujikura can investigate anyhow should be required.

Offered scrap wafers cannot be returned, however the confidentiality of them must be kept and Fujikura should carefully handle them not to flow out of the Fujikura's site very much.

3.1. Wafer Sizes and Thickness

Provided wafers should conform to the SEMI or JEITA standard and its diameter should be 150mm or 200mm.

Please inform the length of the orientation flat or the specification of the index notch to the Fujikura application engineer.

Dice that are located in edge area of wafers wouldn't conform to the required specifications due to non-uniformity of the resin layers.

The current maximum width of the non-conforming area band is 10mm from the wafer edge.

Please consult with the Fujikura application engineer about your acceptable effective area.

Regarding the thickness of the wafer, please check with the Fujikura application engineer.

3.2. Scribe Line

Customers should consider the space margin for chipping that might give damages to the initial resin layer or overcoat when you do the dicing process.

The most outer bump should exist at least a half of the bump pitch off from the inner edge of the scribe line.

In Fujikura wafer level packaging service, no layer is put on the scribe line except the alignment mark.

Please inform the followings in advance.

- Die size (Pattern pitch and formed size after dicing)
- Width of scribe lines
- Dicing space margin for chipping
- The number of dice per wafer

3.3. Passivation Type

Wafer passivation can be oxyside, nitride, oxynitride or PolyImide (PI).

Please provide a few scrap wafers to check the adhesive performance of the initial resin layer against the passivation in advance.

When you use PI for your final passivation, the transparency of the PI is the key factor in Fujikura's processes.

Please inform the transparency and the thickness of the passivation to the Fujikura application engineer.

3.4. Passivation Opening

Please inform the size, the gap and the forming shape of the passivation openings to the Fujikura application engineer in advance.

If there are other passivation openings for memory repair or laser trimming, the opened area treated as a passivation opening on the final metal I/O pads and may be given damage in Fujikura wafer level packaging processes.

If you need special protections for the openings, please check the availability with the Fujikura application engineer.

3.5. Final Metal Pad

Please inform the material, size, pitch and the number of the final metal

I/O pads to the Fujikura application engineer.

The minimum I/O pitch should be 100micron at this moment.

3.6. Maximum Surface Gap

A big gap at the wafer surface may affect the processes.

Please inform the maximum gap depth and aspect ration to the Fujikura application engineer.

3.7. Probed Wafer and Ink Dot

Ink dots on wafer should not be accepted, which may cause problems in the processes.

Probed impressions on the I/O pads are acceptable, which must be small enough and should be checked with the provide scrap wafers.

3.8. Backside Finish

Please inform the specification of the wafer backside finish.

If spot or splash to wafer backside in Fujikura wafer level packaging processes make problems, please let us know in advance.

3.9. ESD

If your dice require special treatments against ESD, please check with the Fujikura application engineer.

4. Alignment Tolerance

Alignments for all photolithography are done by a featured pattern of the final metal layer on the die or in the scribe line, and of which size must be within 75microns.

The tolerance is +/-4microns with an aligner or +/-2microns with a stepper.

If the wafer has other patterns except the objective die such as TEG, please inform it to the Fujikura application engineer in advance.

5. Design Consideration & Package Specification

The followings are design rule details of Fujikura wafer level packaging service.

5.1. Initial Resin Layer

The initial insulation layer is usually made of a photosensitive resin, and

its required thickness is 5microns or more.

If you have special requirements or limits for the material or the thickness, please check with the Fujikura application engineer in advance.

5.2. Resin Post

If you require the resin post underneath the solder bump, the minimum post pitch should be 300microns and the minimum diameter of the post, which is defined at the foot, should be 150microns.

If you have special requirements or limits for the material, height, pitch or diameter of the resin post, please check with the Fujikura application engineer in advance.

5.3. Rerouting

The rerouting is made of electro plated Cu, and its thickness is 5...20microns.

The minimum line & space depends on the post height (wafer roughness) and the thickness of the Cu layer.

For instance, when the post height is 30microns and the thickness is 10microns, the minimum line & space should be 18/18microns.

If you have special design considerations for the material, layout or impedance, please let the Fujikura application engineer know.

5.4. Seed Layer

The seed layer underneath the plated Cu (Rerouting) layer is spattered Cu/Cr. The thickness is controlled in the Fujikura standard process.

If you have special requirement or limit for the material or the thickness, please check with the Fujikura application engineer in advance.

5.5. Solder Bump

Eutectic 63Sn/37Pb solder and Lead Free solder are the standard material for solder bumps in Fujikura wafer level packaging service, which are formed by screen printing method.

Please inform which solder material you choose, the number of bumps, required uniformity, coplanarity, joint condition, joint strength and flux washing requirement

In an actual Eutectic 63Sn/37Pb example, the minimum solder bump pitch

is 300microns and the maximum size is 250microns.

The available solder bump size depends on its pitch distance, and the possible layout is peripheral or array pitch.

Please consult with the Fujikura application engineer about the solder type, forming shape, pitch and layout if you have special requirements or limits.

Fujikura can deliver packaged wafers without solder bumps, and gold plating finish may be required at the overcoat opening where plated Cu layer is bared and possibly oxidized.

Please consult with the Fujikura application engineer about the details of the finish specification.

5.6. Overcoat Resin

Currently a photosensitive resin is used as the overcoat, of which required thickness is 10microns minimum.

If you have special requirement or limit for the material or the thickness, please check with the Fujikura application engineer in advance.

6. Test & Inspection

The followings are test & inspection specifications of the Fujikura wafer level packaging service.

Sampling should be specified properly at the development stage, the pre-production stage and the high volume production stage respectively.

Please check with the Fujikura application engineer about the sampling.

6.1. Visual Inspection

Sampling visual inspection for the pattern or the form should be done at wafer level or die level.

Please check with the Fujikura application engineer about the sampling rate and criteria.

6.2. Bump Inspection

Basically sampling bump inspections should be done in the bump height, size, strength (peel and shear), coplanarity and so on.

Please check with the Fujikura application engineer about the sampling

rate and criteria.

6.3. Reliability Test

Wafer level, components level after the dicing or board level (solder joint) reliability tests must be done and evaluated.

Please check with the Fujikura application engineer about testing items, conditions and sampling rate.

7. Packing

Packing specifications for returning packaged wafers is same ones for provided wafers from customers.

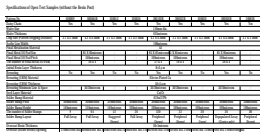
Vacuum or Nitrogen sealed packing aren't available at this moment.

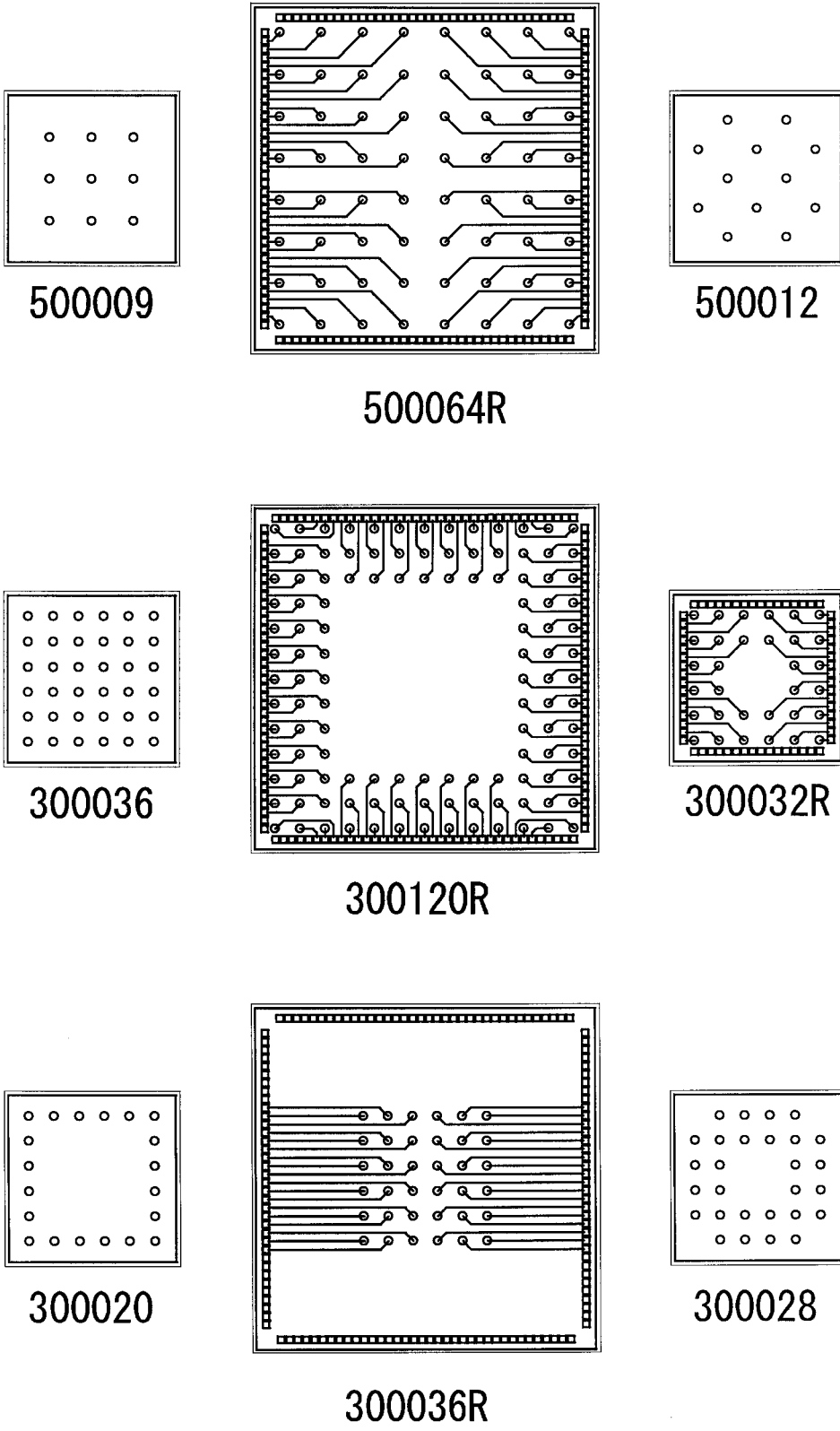
Please consult with the Fujikura application engineer about the packing specification.

Appendix1 Fujikura Wafer Level CSP Specification Chart (Click to open the file)

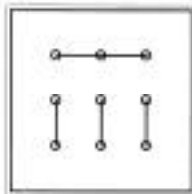


Appendix2 Specification & Pattern of Open Test Samples (without the Resin Post) (Click to open the file)

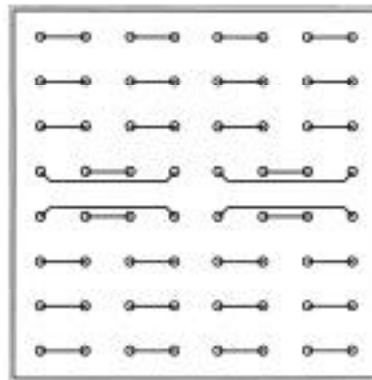




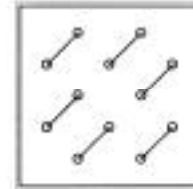
Solder bump layout and rerouting pattern of Open Test Samples (without the Resin Post)



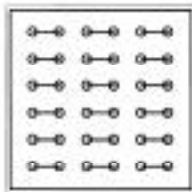
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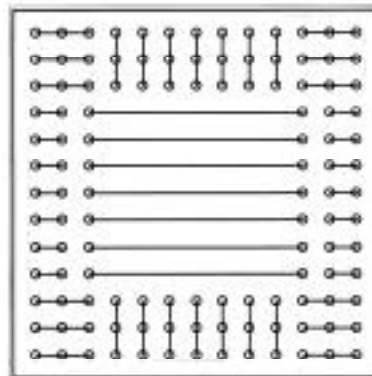
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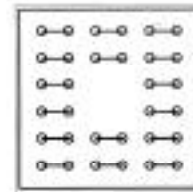
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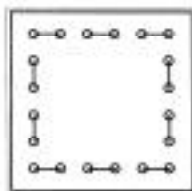
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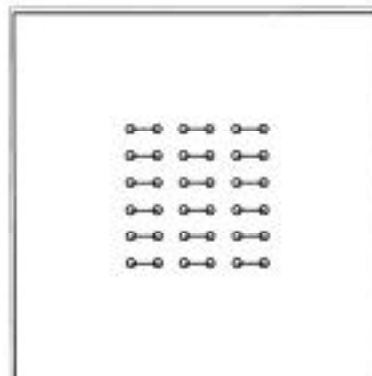
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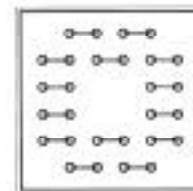
300032R



300020

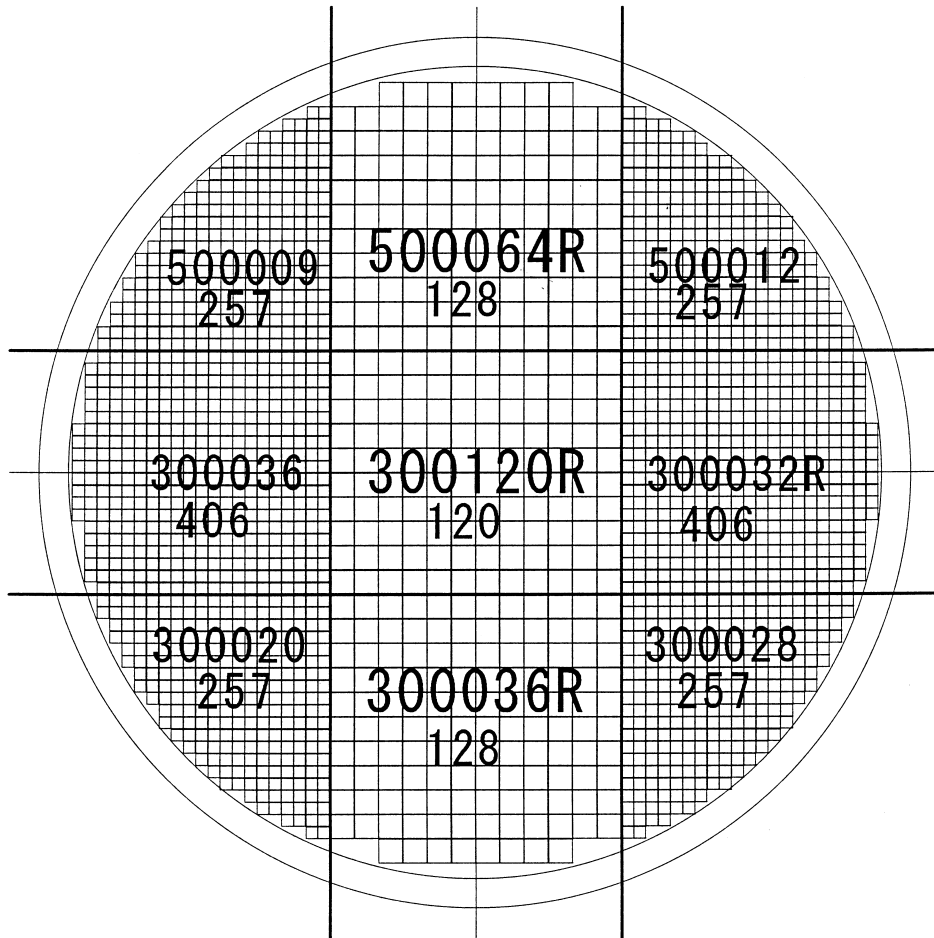


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Daisy chain pattern of Open Test Samples (without the Resin Post)



Wafer mapping of Open Test Sample (without the Resin Post)